

## CLAIMS

### What is claimed is:

1. An circuit for disabling a pull-up resistor connected to a data line of a universal serial bus device, comprising:  
a universal serial bus connection comprised of at least one power source and at least two data lines;  
an integrated circuit connected to the at least two data lines and having an input;  
an external power supply connected to the integrated circuit;  
at least one transistor interconnected between VBUS and the input, the power source and the integrate circuit for controlling voltage to the input of the integrated circuit corresponding to the voltage of VBUS; and  
a pull-up resistor connected between the application specific integrated circuit and a data line of a USB connection, the state of the pull-up being controlled by the application specific integrated circuit depending upon the voltage on the input.
2. The circuit of claim 1, wherein said at least one transistor has a base, a collector and an emitter, the power source

connected to the base, the external power supply connected to collector and the emitter connected to the integrated circuit.

3. The circuit of claim 2, further including at least one first resistor interposed between the power source and the base of the at least one transistor to drop the voltage of the power source before being applied to the base of the at least one transistor.

4. The circuit of claim 3, further including a second resistor connected to ground and to the emitter of the at least one transistor and a first pull-up resistor connected between the external power supply and the emitter of said at least one transistor.

5. The circuit of claim 4, wherein the power source is at approximately 5 volts, the external power supply is at approximately 3.3 volts, the first resistor is an approximately 121 k $\Omega$  resistor, the second resistor is an approximately 2.49k $\Omega$  resistor, and the transistor is a Q2N2222 transistor.

6. The circuit of claim 1, wherein said resistor comprises an NPN bipolar junction transistor.

7. The circuit of claim 1, further including circuitry for providing hysteresis to filter noise from the external power supply.

8. The circuit of claim 7, wherein the circuitry for providing hysteresis comprises an input buffer through which voltage on the input is buffered.

9. The circuit of claim 4, further including an electrostatic protection diode in parallel with the first pull-up resistor, the transistor protecting the electrostatic protection diode from voltage from the power source.

10. The circuit of claim 1, wherein relatively little current is drawn from the power source when the external power supply is at zero.

11. The circuit of claim 1, further including a logic circuit within the integrated circuit.

12. The circuit of claim 11, wherein said logic circuit is a universal serial bus to ATAPI bridge.

13. The circuit of claim 11, wherein said application specific integrated circuit provides an AND gate function for allowing current to flow to the pull-up resistor if the voltage on the input represents a logic one.

14. The circuit of claim 11, wherein a logic one will be present if the input is above about 2.7 volts and a logic zero will be present if the input is below about 2.2 volts.

15. A method of disabling a pull-up resistor connected to a data line of a universal serial bus device comprising a universal serial bus connection comprised of a power source, at least two data lines, a pull-up resistor connected to one of the at least two data lines, an external power supply and an integrated circuit having an input, the method comprising:

detecting the presence of a voltage of the at least one power source;

applying a voltage to the input of the integrated circuit that is proportionate to the voltage on the at least one power supply;

determining if the voltage on the input represents a logic one or a logic zero; and

enabling the pull-up resistor if the voltage on the input

represents a logic one and disabling the pull-up resistor if the voltage on the input represents a logic zero.

16. The method of claim 15, further including preventing the pull-up resistor from alternating from enabled to disabled due to noise in a signal from the external power supply.

17. The method of claim 16, further including buffering the external power supply voltage to provide hysteresis for filtering noise.

18. The method of claim 15, further including providing at least one transistor interconnected between the power source and the integrate circuit for controlling voltage on the input of the integrated circuit.

19. The method of claim 18, further including dropping the voltage of the power source before applying the voltage to the base of the at least one transistor.

20. The method of claim 15, further including configuring the integrated circuit as a universal serial bus to ATAPI bridge.

21. The method of claim 18, further including providing the integrated circuit with an electrostatic protection diode and protecting the electrostatic protection diode with the at least one transistor.

22. The method of claim 15, further including drawing relatively little current from the power source when the external power supply is at zero.

23. The method of claim 15, wherein said determining if the voltage on the input represents a logic one or a logic zero is performed by providing an AND gate function between the input of the integrated circuit and the pull-up resistor such that the AND gate function will allow current to flow through the pull-up resistor if a logic one is present.

24. The circuit of claim 23, further including enabling the pull up resistor if the power source is above about 2.7 volts and

disabling the pull-up resistor if the power source is below about 2.2 volts.

25. A method for preventing malfunctions in a data transmission system which transmits digital signals along a data bus between a host computer and a peripheral device wherein the peripheral device may receive power from the host computer or alternatively from an external power source, comprising

interconnecting a transfer bridge circuit between the host computer and the peripheral device, the bridge circuit having a first interface between the bridge circuit and the host computer, a second interface with a protective circuit, and a third interface with the peripheral device electronics,

providing a pull-up resistor connected in a separate line between the first interface and the data bus,

sensing whether power is being supplied along a power line from the host computer to the peripheral device, and if appreciable power is not detected in the host power line, then

deactivating the pull-up resistor to prevent any malfunction from occurring.

26. The method of claim 25 wherein said deactivating occurs upon sensing that a voltage in the host power line is below a predetermined first threshold level

27. The method of claim 26 which further includes activating the pull-up resistor upon sensing that a voltage in the host power line is above a predetermined second threshold level.

28. The method of claim 27 wherein said second threshold level is higher than said first threshold level

29. The method of claim 25 which further includes providing an input line to the second interface from an electronic gate coupled to the power line, and incorporating a logic circuit in the bridge circuit connected to the second interface, and generating a logical I/O control signal from the logic circuit to cause the enabling or disabling of the pull-up resistor.

30. The method of claim 29 wherein said input line is capable of creating three different states of operation in the bridge circuit, including a first state when an external power supply is connected to the peripheral device with the pull-up resistor disabled.

31. The method of claim 30 wherein the data bus incorporates two transmission lines each capable of transmitting data at different rates, respectively, and including a second state when the host computer supplies power to the peripheral device with the pull-up resistor enabled